Analysis of the µPD650C-133 CPU timing

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This paper discusses the timing of the µPD650C-133 CPU used in the Roland TB-303 synthesizer. The original part was connected to a Saleae logic analyzer and various patterns have been analyzed to get an exact idea of the timing used for gate, accent and slide signals generated by the 303 sequencer. The findings of clock latency, impulse length and jitter are discussed and the measurement data is analyzed. The data shows that the gate signal not a static value tied to the tempo clock and is under constant flux due to beating between the tempo clock and the CPUs external interrupt clock. Other signals as slide and accent are tied to the gate signal and show the same timing fluctuations as the gate signal.

0 INTRODUCTION

A lot of information about the inner workings of the 303 sequencer can be found on the internet [1], [2], but the accuracy is sometimes questionable. To shed some light on the timing of the original µPD650C-133 CPU and end the speculations and misinformation exact measurements were needed. In this paper we discuss the findings of analyzing an original CPU. While taking measurements, it became clear that the TB-303 has some properties that deviate from an ideal theoretical timing, that are somewhat relevant to its characteristic sound.

1 HARDWARE

The µPD650C-133 is a mask ROM CPU manufactured by NEC, the CMOS version of the a µCOM-43 microcomputer. It supports a maximum clock frequency of 440kHz.[5]

The interrupt of the processor is controlled by the falling edge of an external oscillator and executed every 1.8ms[3].

2 CLOCK

The DIN sync clock utilized a 24ppq resolution. The tempo clock is generated by an external oscillator circuit. If the TB-303 is synced to other gear via the DIN sync jack on the back, a switch in the DIN jack replaces the internal clock and start/stop signal with the clock coming from the external gear. The clock properties are unaffected as both clock sources follow the DIN sync specification found in the TR-808 service manual[4].

3 SIGNAL LATCHING

The note bit values for the R2R DAC and the accent signal are latched through buffer ICs by the slide signal. That means that a new note and an accent have to be set by the CPU before the slide signal activates them for the subsequent circuitry. It also means that no new note or accent value can be set without a short activation of the slide signal. When no slide is applied to a new note, the slide circuitry is still active for about 44µs at the beginning of each new note. The latch also synchronizes the accent and note signals.

Fig. 1. Latch pulse on the slide signal at the beginning of a non slid note.

4 GATE

The first thing obvious from the measurement data is that the CPU does not react immediately to incoming tempo clock pulses. A latency between 0.8ms and 3.3ms between the rising edge of the tempo clock signal and the subsequent rising edge of the gate signal was observed in the data. The standard deviation in the data for the gate on delay is 0.74ms with a mean value of 2.06ms.

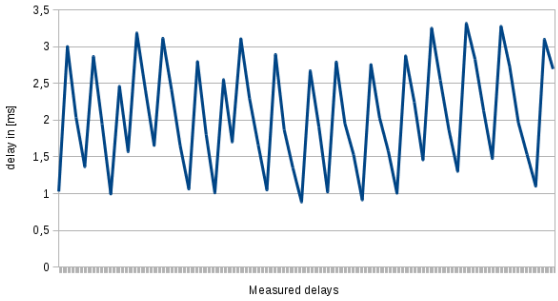

Fig. 2. Delay between the rising edge of the clock and gate signal at medium tempo.

Since the jitter varies from gate to gate, the assumption was made that it has to do with the interrupt routine that is not synced to the tempo clock.

At first, it was not clear if timing jitter is due to the interrupt delaying the clock while the ISR has to be processed to read and set panel control settings or if the clock signal itself is handled in the ISR.

No information was found about the processing times and tasks handled in the TB-303 ISR, but a look at the TR-808 service manual can clarify some observations.

In the service notes of the TR-808, which uses the same processor family, a bit more information is given and it is assumed that similar values are utilized on the TB-303. The 808 has an interrupt every 1.9ms, and the complete ISR takes about 600µs[4]. So the rest of the time between interrupt signals is left for the main program handling. The 808 ISR handles the reading of switches and buttons of the user interface, as well as handling all of the LEDs. It is also mentioned in figure 2, the interrupt cycle diagram, that the tempo clock and start/stop signal is processed inside the ISR[4].

Further measurements on the TB-303 confirm this to be true for the 303 as well. Looking at the delay times between the falling edge of the interrupt clock and the rising edge of the following gate signal, we have a latency of about 0.917ms to 1.062ms in the test data. This is a much more consistent value than the wildly varying relation between tempo clock and gate signal and we can conclude that it takes about 1ms for the gate signal to become high after the first interrupt clock when a new note has to be played.

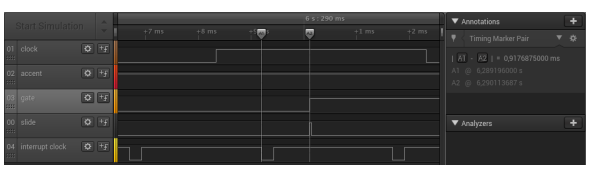

Fig. 3. Latency between interrupt clock and gate on.

The same applies to the gate off delay, albeit with a different latency. The measured data suggest a gate off latency between the interrupt clock and the falling edge of the gate signal of approximately 2.3ms to 2.4ms.

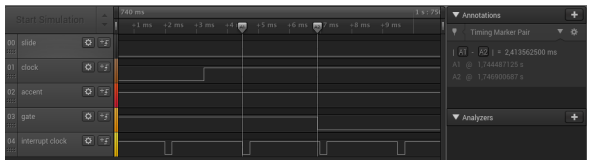

Fig. 4. Latency between interrupt clock and gate off.

The delay between the falling edge of the tempo clock and the falling edge of the gate signal in the measured data is between 2.25ms and 5.45ms with a standard deviation of 0.75ms and a mean value of 3.51ms.

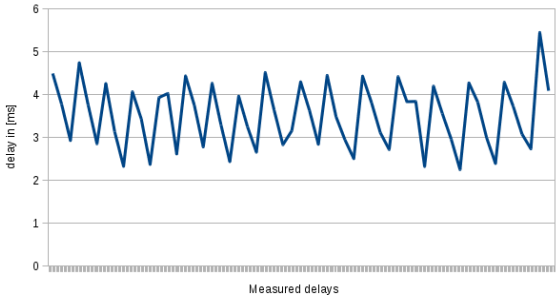

Fig. 5. Delay between the falling edge of the clock and gate signal at medium clock tempo.

These small delays are inaudible for most ears. A study conducted by the AES concludes that a musician will probably not notice any delay for latencies smaller than 6.5ms[6]. Nontheless it is important if the goal is to recreate an exact copy of the original TB-303 timing. This becomes also apparent if a simple 16th note pattern is programmed on the TB-303. Especially with higher speeds, a slight beating in the note accentuation can be heard.

The interplay of the two clocks also results in slightly different note lengths

4.1 4/4 mode

In the normal mode the 303 operates in a 4/4 measure. At 24ppq that equals 6 clock pulses per step. The on/off duty cycle for the gates is 3 clocks on and 3 clocks off. The theoretical duty cycle is 50 %, but the measurements show that the 303 has a slightly longer on than off time that is dependant on the interrupt clock and its beating with the tempo clock. Thus the gate lengths are under a constant variation up to several ms and random examination of the measured data suggests duty cycles between 49.96% and 55.8%.

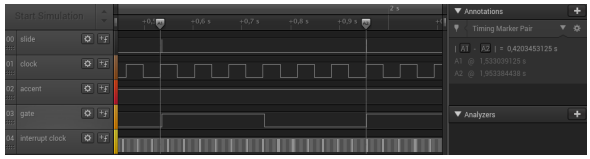

Fig. 6. Step duration of 6 clocks. 3 clocks on and 3 clocks off.

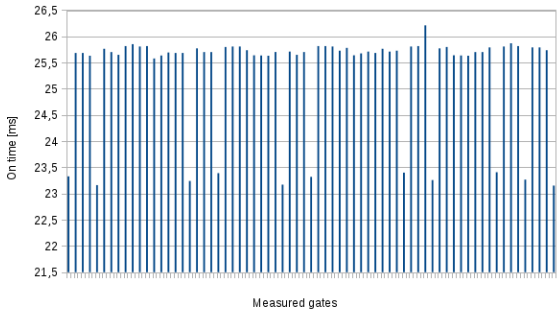

Fig. 7. Gate on times at fast tempo.

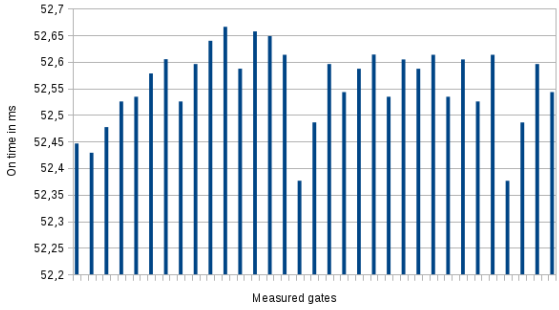

Fig. 8. Gate on times at medium tempo.

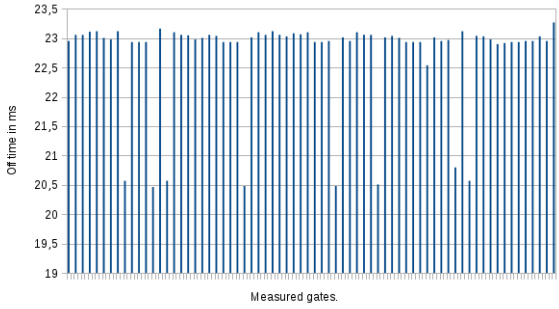

Fig. 9. Gate off times at fast tempo.

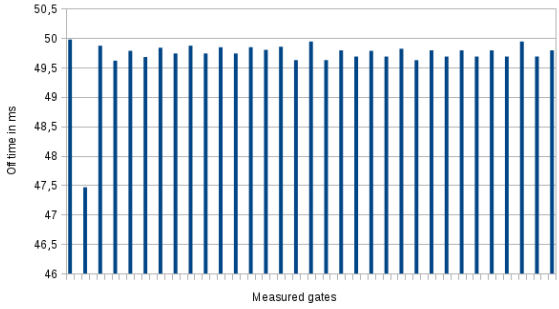

Fig. 10. Gate off times at medium tempo.

4.2 Triplet mode

In triplet mode the 303 operates on a 3/4 measure. At 24ppq the gate duration is 8 clock pulses per step. The on/off duty cycle for the gates is 5 clocks on and 3 clocks off, resulting in an asymmetrical on/off ratio. Gate on/off latency is the same as in the 4/4 measure mode.

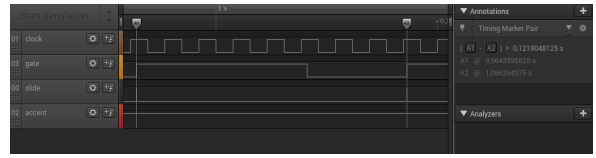

Fig. 11. Step duration of 8 clocks for triplet mode. 5 clocks on and 3 clocks off.

4.3 Gate behaviour on slide notes

The gate is not turned off if the next note in a sequence has the slide attribute activated.

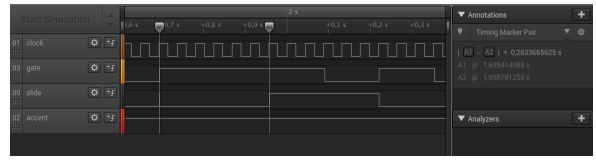

Fig. 12. The gate stays high if the next note has an active slide.

5 ACCENT

The accent signal is quite simple, it is high for 2 of the 3 clock pulses of a 4/4 measure gate on period. A large number of stray pulses are present in the gate signal during the off state.

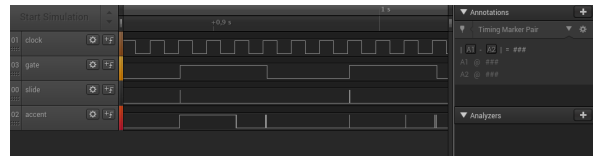

Fig. 13. Non latched accent signal with stray pulses.

Since the accent is latched by the flip-flop IC13, it is synchronized to the whole step duration and exactly as long as a complete gate on/off cycle. Stray pulses are ignored.

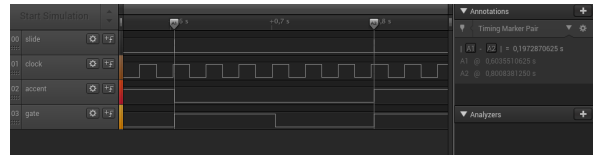

Fig. 14. Latched accent synchronized to the gate signal. Inverted signal since measurements were taken on the $\overline{Q}$ gate of the flip-flop.

For ties, rests, and 2 accented notes after one another, the accent behaviour is quite deterministic since it simply stays active over the whole duration and is turned off at the beginning of the next unaccented note.

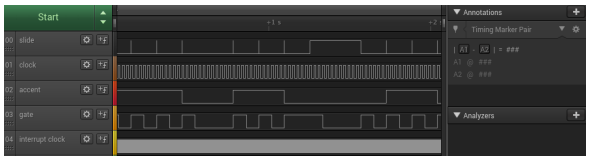

Fig. 15. First accent is followed by a rest. Second accent is followed by a tie and rest, with the following step accented as well.

6 SLIDE

Two things happen if the slide attribute is set on a step. As mentioned in 4.3, the gate stays high in front of a slid step. The slide signal itself is set high at the beginning of the slid step. Since the slide signal also latches the note signal to the R2R DAC, the positive edge of the slide signal is synchronized to the beginning of a new note. It turns off after the on/off cycle of the active step is completed at the beginning of the next non slid step.

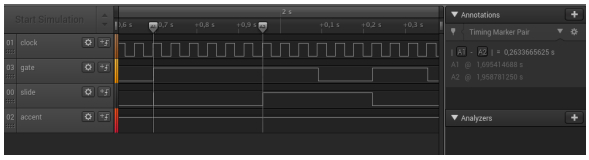

Fig. 16. The slide is activated on the beginning of the slid step.

The slide signal seems to be always high during tie and the following rest steps. No pitch value change occurs during this time and it has no effect on the generated pitch CV.

Fig. 17. The slide signal is high during ties and rests even if no slide attribute was set.

During slides that span multiple different notes, the slide is pulled low for 8.75µs to latch a new note to the DAC.

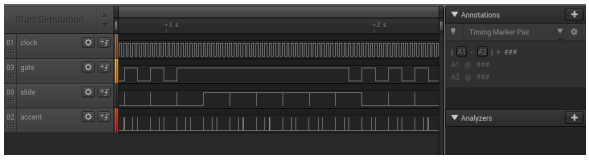

Fig. 18. The slide signal is pulled low on every new note to latch the new value into the DAC.

Fig. 19. Closeup of the 8.75µs slide latch.

7 TEMPO INFLUENCE

Tempo influence on the latency could not be measured. Differences between slow and fast tempo clock settings stay in the normal variations that were also observed within a data array taken from an unchanged tempo clock.

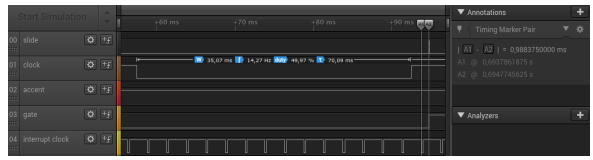

Fig. 20. Gate on latency on slow tempo clock speed = 0.998ms.

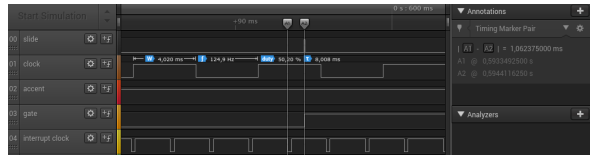

Fig. 21. Gate on latency on fast tempo clock speed = 1.062ms.

The audible result varies with different tempo clocks since the latency is a fixed value. A 2.4ms gate off delay has nearly no impact on the perceived sound when a step takes nearly half a second like on the slowest possible tempo clock setting. The duty cycle difference is below 1% (random data samples suggest 50.25% to 50.5% duty cycle). With the fastest tempo clock a complete step takes only 50ms resulting in duty cycles up to 55% to 56% which are much more audible.

The interplay of the clocks is another factor much more relevant to the speed of the tempo clock. The interrupt clock is fixed at 1.8ms, therefore the beating pattern with the tempo clock is highly dependant on the set tempo. If the tempo clock is set to multiples of the interrupt clock there is no beating. For example 278 interrupt clocks at 1.8ms each equals a tempo of 119.90 BPM.

$$\frac{60sec}{278 * 1.8ms} = 119.90BPM \tag{1}$$

8 CONCLUSION

The interaction of different clock sources and processing times in the interrupt routine in the digital section of the TB-303 brings a noticeable amount of fluctuations to the timing of the TB-303 sequencer. Even if the nuances are small, an emulation of the original TB-303 can not claim to be complete without taking these variations into consideration.

9 ACKNOWLEDGMENT

This research was conducted in spring 2017 as a part of the development of the RE-303 CPU, a replacement CPU for a true to the original TB-303 replica. It was only made

possible due to the generous loan of an original μPD650C-133 CPU by Andreas Kump. The author would also like to thank Paul Barker for the time and energy he put into the RE-303 project and his meticulous recreation of the TB-303 PCBs. Also many thanks to Robin Whittle who has put a lot of useful information regarding the 303 on his Devil Fish website. The Roland Corporation was in no way involved in the RE-303 project, but a big thank you goes out to them for the creation of the wonderful TB-303 that inspired so many of us. Technical editing, language editing, and proofreading was done by Raph Wlodarczyk.

10 REFERENCES

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[3] Roland, "TB-303 Service Notes (First Edition)," (Japan, 1982).

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[5] NEC Microcomputers, Inc., "μCOM-43 Users' Manual," (NEC Microcomputers, Inc. 1978).

[6] Lester et al, "The Effects of Latency on Live Sound Monitoring," (Convention Paper presented at the AES 123rd Convention, New York, NY, USA, 2007 October 58), page 19.

NOMENCLATURE

ISR = Interrupt service routine
DAC = Digital analog converter
R2R = An R2R Ladder is a simple and inexpensive way to perform digital-to-analog conversion, using repetitive arrangements of precise resistor networks in a ladder-like configuration.